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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,128	03/29/2004	Thomas T. Hardt	200311280-1	2179

22879 7590 10/16/2006

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EXAMINER	
WRIGHT, INGRID D	

ART UNIT	PAPER NUMBER
2835	

DATE MAILED: 10/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,128	HARDT ET AL.	
	Examiner	Art Unit	
	Ingrid Wright	2835	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-15 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-15 and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/29/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *2 Attachments*.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3,5-15, & 17-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roscoe et al. US 6498731 B1 in view of Wallace et al. US 6628537 B1, further in view of Baker et al. US 6819567 B2. Note: See attached fig. 9 of Roscoe et al., fig. 3 of Baker et al.

With respect to claim 1, Roscoe et al. teaches a memory package (see, Abstract of Roscoe et al.) comprising a first cover portion (264), a first electronics sub-assembly (see, fig. 9 of Roscoe et al.) that comprises a first circuit board (268) with at least one memory module socket (see, fig. 9 of Roscoe et al.) projecting from a surface of the first circuit board (268), and at least one controller chip coupled to a processor (22) and mounted on the circuit board (268), wherein said first electronics sub-assembly is supported by the first cover portion (264), a second cover portion (262) connected to said first cover portion (264), a second electronics sub-assembly (see, fig. 9 of Roscoe et al.) that comprises the circuit board (268) with at least one memory socket (see, fig. 9 of Roscoe et al.) projecting from a surface of the circuit board (268), and at least one controller chip coupled to the processor (22) and mounted on the circuit board (268), wherein the electronics sub-assemblies (see, fig. 9 of Roscoe et al.) is supported by said second cover portion (262), wherein said first and second cover portions (264,262) are moveable between a closed position wherein said electronics sub-assemblies are nested, but is silent as to the

memory module socket mounted on the circuit board (268) is in an opposed relationship with an adjacent controller chip mounted to a second circuit board and a memory module socket mounted to a second circuit board is in an opposed relationship with a controller chip mounted to a first circuit board.

Wallace et al. teaches controller chips (13) mounted on a circuit board (11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the controller chip, as taught by Wallace et al. in the invention of Roscoe et al., in order to provide an independently operable controller chip board assembly.

Baker et al. teaches a circuit board (110), comprising an electronics assembly (105), within a first and a second cover portion (see, fig. 3 of Baker et al.) of an expansion unit (120), for providing expansion components for a blade (see, Abstract of Baker et al.).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize an electronics assembly mounted on a second cover portion as taught by Baker et al., in the invention of Roscoe et al., in order to provide expansion components for the protective assembly of Roscoe et al.

As to the placement of the boards, Roscoe et al. as modified Wallace et al & Baker et al., teaches a memory module socket (see, fig. 9 of Roscoe et al.) mounted on a circuit board (268), comprising a plurality of usable slots and a controller chip (coupled to a processor (22)), further mounted on the circuit board (268) and a second circuit board (110), except wherein the memory module socket mounted to a

circuit board, and a memory module socket mounted to a second circuit board in an opposed relationship with an adjacent controller chip mounted on a first circuit board.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to place the controller chip of Wallace et al. in a slot adjacent to a memory module socket of Roscoe et al., in order to provide an alternate equivalent board arrangement of a controlled circuit system.

With respect to claim 2, Roscoe et al. teaches (Fig. 2) first and second cover portions (264, 262) further comprises a base surface and wherein when said cover portions (264, 262) are in the closed position, the base surfaces of said cover portions (264, 262) face each other.

With respect to claim 3, Roscoe et al. teaches (Fig. 2) the circuit boards (210) of said first and second electronics sub-assemblies are positioned substantially parallel to and offset from each other. when said first and second cover portions are in the closed position.

With respect to claim 5, Roscoe et al. teaches (Fig. 9) each of said first and second cover portions (264,262) further comprises a base surface and said cover portions (264,262) have an open position wherein the base surfaces of said cover portions (264,262) do not face each other.

With respect to claim 6, Roscoe et al. teaches (Fig. 9) the circuit boards (210) of said first are positioned substantially parallel to and substantially co-planar with each other when said first and second cover portions (264,262) are in the open position.

With respect to claim 7, Roscoe et al. teaches (Fig. 9) a hinge (278) pivotally connecting said first cover portion (264) and said second cover portion (262).

With respect to claim 8, Roscoe et al. teaches (Fig. 9) a latch (282) operable to retain said cover portions (264,262) in the closed position.

With respect to claim 9, Roscoe et al. teaches (Fig. 9) an electrical connector (216) operable to couple said electronic sub-assemblies to a processor- based device.

With respect to claim 10, Roscoe et al. teaches (Fig. 9) an electronic sub-assembly further comprises an electrical connector (216) operable to couple one electronic sub-assembly to a processor-based device.

With respect to claim 11, Roscoe et al. teaches (Fig. 9) a handling aperture (288) in at least one of said cover portions (264).

With respect to claim 12, Roscoe et al. teaches (Fig. 2, 9) the circuit board (210) of said first electronics assembly identical to the circuit board (210) of said second electronics assembly.

With respect to claim 13, Roscoe et al. teaches (Fig. 9) a plurality of memory modules (206) received by the memory module sockets.

With respect to claim 14, Roscoe et al. teaches a processor (22), a chassis supporting said processor (22) and a memory package (see, fig. 9 of Roscoe et al.) comprising, an electronics assembly (see, fig. 9 of Roscoe et al), comprising a circuit board (268), wherein the circuit board (268) is coupled to at least one

memory module (see, fig. 9 of Roscoe et al.) and at least one memory controller coupled to , and a housing assembly ( ) supporting said electronics assembly, wherein said housing assembly ( ) has a first cover portion (264) supporting the circuit board (268) and a second cover portion (262); wherein said memory package has a closed position and an open position, wherein in the closed position said housing engages said chassis (248) and said electronics assembly electrically couples with said processor (22), and a memory controller, coupled to a processor (22) and mounted on a first and second circuit board (210,210).

Roscoe et al. is silent as to a controller chip mounted on an individual board and a second cover portion supporting a second circuit board.

Wallace et al. teaches controller chips (13) mounted on a board (11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the controller chips, as taught by Wallace et al. in the invention of Roscoe et al., in order to provide an independently operable controller chip board assembly.

Baker et al. teaches a second cover portion (see, fig. 3 of Baker et al.) supporting a circuit board (110), of an expansion unit (120).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the second cover portion and assembly/board arrangement as taught by Baker et al., in the invention of Roscoe et al., in order to provide expansion components for a blade (see, Abstract of Baker et al.).

As to the placement of the boards, Roscoe et al. teaches a memory module socket (208) mounted on a first circuit board (210) and a plurality of usable slots, a second memory module (208) socket mounted on a second circuit board (210), and a controller chip (22) (coupled to a processor on a first and second circuit board (210,210)), except wherein the memory module socket on a first circuit board is placed adjacent a controller chip mounted on a second board, and a memory module socket on a second board is placed adjacent a controller chip mounted on a first circuit board.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to place the controller chip of Wallace et al. in a slot adjacent to a memory module socket of Roscoe et al., in order to provide an alternate equivalent board arrangement of a controlled circuit or system.

With respect to claim 15, Roscoe et al. teaches (Fig. 2,9) the first and second circuit boards (210) are positioned substantially parallel to and offset from each other when said memory package is in the closed position.

With respect to claim 17, Roscoe et al. teaches memory package has an open position wherein said housing is disengaged from said chassis and said electronics assembly is decoupled from said processor.

With respect to claim 18, Roscoe et el. teaches the first and second circuit boards (210) are positioned substantially parallel to and substantially co-planar with each other when said memory package is in the closed position.

With respect to claim 19, Roscoe et al. teaches the electronics assembly further comprises at least one electrical connector (214) coupled to the first and second circuit boards, wherein the at Ieast one electrical connector (214) couples the electronics assembly to said processor.

With respect to claim 20, Roscoe et al. teaches (Fig. 9) the housing assembly further comprises a hinge (278) pivotally connecting the first cover portion and the second cover portion.

With respect to claim 21, Roscoe et al. teaches (Fig. 9) the housing assembly further comprises a Iatch (282) operable to retain said cover portions in the closed position.

With respect to claim 22, Roscoe et al. teaches (Fig. 9) a memory package comprising a means for housing (260) a first and second electronics sub-assemblies (274), daughterboards with memory modules (272), wherein each sub-assembly (274) has at Ieast one memory module (272); means for moving (278,280) at least a portion of said means for housing (260) between an open position allowing access to the memory modules (272) and a closed position where the two electronics sub-assemblies (274) are nested together.

Although, Roscoe et al. teaches a processor (22) coupled with a control circuitry, however it is unclear if a controller chip is on the daughter boards or not.

Wallace et al. is relied upon to show evidence of multiple memory modules with independent control circuitry, via controller chips (13) mounted on a circuit board (11) (see, fig. 9 of Wallace et al.).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide memory modules of Roscoe et al., with control circuitry such as a controller chip to allow the boards to function independently in view of the teachings of Wallace et al. and Baker et al.

As to the placement of the boards, Roscoe et al. teaches a memory module socket (272) mounted on a first electronic sub-assembly (274), a plurality of usable slots, a memory module socket (272) mounted on a second electronic sub-assembly (274), first and second sub-assembly) (274)), except wherein the memory module socket mounted on a first electronic sub-assembly is placed adjacent a controller chip mounted on a second electronic sub-assembly, and a memory module socket mounted on a second electronic sub-assembly is placed adjacent a controller chip mounted on a first electronic sub-assembly.

It would have been obvious to place the controller chip mounted on the electronic sub-assembly of Wallace et al. adjacent the memory module socket mounted on the electronic sub-assembly of Roscoe et al. and to place a second memory module socket mounted on a second electronic sub-assembly of Roscoe et al. adjacent the controller chip mounted on a first electronic sub-assembly of Wallace et al., in order to provide an alternate equivalent arrangement of a controlled circuit or system.

With respect to claim 23, Roscoe et al. teaches (Fig. 9) means for coupling (278,280) the first and second electronics sub-assemblies (274) to a processor-based device when said means for housing (260) is in the closed position.

With respect to claim 24, Roscoe et al. teaches (Fig. 9) means for retaining (278,280) said means for housing (260) in the closed position.

Response to Arguments

2. Applicant's arguments, filed 7/10/06, have been fully considered, but are not persuasive.

With respect to Applicant's argument #1, regarding Roscoe et al., Wallace et al. or Baker et al., not teaching of at least one memory module socket projecting from a surface of a first circuit board or a second circuit board, the Examiner notes that Roscoe et al. teaches at least one memory module socket projecting from a circuit board, but lacks a second memory module socket projecting from a second circuit board. Further, Baker et al. is relied upon to teach electronic components, mounted on a first and second circuit board mounted, within a first and second cover portion ( ) of a expansion unit (120) and Wallace et al. is relied upon to teach controller chip (13) mounted on a circuit board (11).

As to the controller chip and memory module socket, it would have been obvious to place the controller chip (13) of Wallace et al. on the first circuit board of Roscoe et al., as modified by Baker et al., as it is well known in the art for motherboards to have controller chips. Further, placing the controller chip of Wallace et al. adjacent a memory module socket of Roscoe et al. as modified by Baker et al., enables the controller chip to be supported by a first and second cover portion of Roscoe et al. as modified by Baker et al. and furthermore, the memory module socket can be placed in an opposed relationship by one of ordinary skill, with an adjacent controller chip supported by the second cover of Roscoe et al., as modified by Baker et al.

With respect to Applicant's argument #2, regarding Roscoe et al. not teaching a memory module socket projecting from a surface of a circuit board, the Examiner respectfully disagrees and notes that Roscoe et al. teaches a memory module socket (216) projected from a circuit board (218), as shown in fig. 9 of Roscoe et al.

With respect to Applicant's argument #3, regarding Roscoe et al. not teaching a memory module socket mounted to a first circuit board (which is part of a first electronics sub-assembly supported by a first cover portion being in an opposed relationship with an adjacent controller chip mounted to a second circuit board (which is part of a second electronics sub-assembly by a second cover), the Examiner notes that Roscoe et al. teaches a plurality of memory module sockets (216) mounted on a circuit board (218), which comprises two electronic assemblies (see, fig. 9 of Roscoe et al.) and two cover portions (264,262), wherein the first and second electronic sub-assemblies (see, fig. 9 of Roscoe et al.) are supported by the first cover (262), but details that Roscoe et al. is silent as to the second electronic sub-assembly mounted on a second circuit board of the second cover portion. Further, the Examiner notes that Baker et al. is relied upon to teach a first and second circuit board, comprising electronic components, mounted on a first and second cover portion (see, fig. 3 of Baker et al.) of a expansion unit (120) and Wallace et al. is relied upon to teach a controller chip (13) mounted on circuit board (11).

As to the controller chip, it would have been obvious to place the controller chip (13) of Wallace et al. on the first circuit board of Roscoe et al., as modified by Baker et al., as it is well known in the art for motherboards to have controller chips. Further, placing the controller chip of Wallace et al. adjacent a memory module socket of Roscoe et al. as modified by Baker et al., means the controller chip can be supported by a first and second cover portion of Roscoe et al. as modified by Baker et al. and furthermore, the memory module socket can be placed in an opposed relationship by one of ordinary skill, with an adjacent controller chip supported by the second cover of Roscoe et al., as modified by Baker et al.

With respect to Applicant's argument#4, that there is no suggestion to combine the references, the Examiner recognizes that references cannot be arbitrarily combined and that there must be some reason why one skilled in the art would be motivated to make the proposed combination of primary and

secondary references. In re Nomiya, 184 USPQ 607 (CCPA 1975). However, modification be expressly articulated. The test for combining references is what the combination of disclosures taken as a whole would suggest to one of ordinary skill in the art. In re McLaughlin, 170 USPQ 209 (CCPA 1971). References are evaluated by what they suggest to one versed in the art, rather than their specific disclosures. In re Bozek, 163 USPQ 545 (CCPA) 1969. Also, the Examiner clarifies that the claims were viewed as a whole and each limitation of the claims were considered in determining the patentability of the Applicant's claims.

With respect to Applicant's argument#5, regarding Roscoe et al. not teaching a memory module projecting beyond a memory controller, the Examiner notes that Roscoe et al. teaches a memory module (210), located in memory module socket (216), which is projected from a circuit board (218) and a controller chip coupled to a processor (22), Wallace et al., but is silent as to a memory controller chip supported by a second cover portion and a memory module supported by a first cover portion opposing a memory controller. Further, the Examiner notes that Baker et al. is relied upon to teach electronic components, mounted on a first and a second circuit board (110), within a first and second cover portion (see, fig. 3 of Baker et al.), of a expansion unit (120) and Wallace et al. is relied upon to teach controller chip (13), mounted on a circuit board (11). Furthermore, the memory module socket can be placed in an opposed relationship by one of ordinary skill, with an adjacent controller chip supported by the second cover of Roscoe et al., as modified by Baker et al., as memory modules, such as DRAMs and SRAMs, utilizes memory controller chips to access their respective ports or pins.

With respect to Applicant's argument #6, regarding Roscoe et al. not teaching a memory module projecting beyond a memory controller chip, the Examiner notes that Roscoe et al. teaches a memory module (see, fig. 9 of Roscoe et al.) coupled to a controller or processor (22), but is silent as to the

memory module projecting beyond a controller chip. Further, the Examiner notes that Wallace et al. is relied upon to teach a controller chip (13) mounted on circuit board (11). It would be well within the skill of one having ordinary skill in the art, to place the controller chip within the package of Roscoe et al., as memory modules, such as DRAMs and SRAMs, utilizes memory controller chips to access their respective ports or pins.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ingrid Wright whose telephone number is (571)272-8392. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynn Feild can be reached on (571)272-2800, ext 35. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IDW

LYNN FEILD
SUPERVISORY PATENT EXAMINER

FIG. 3

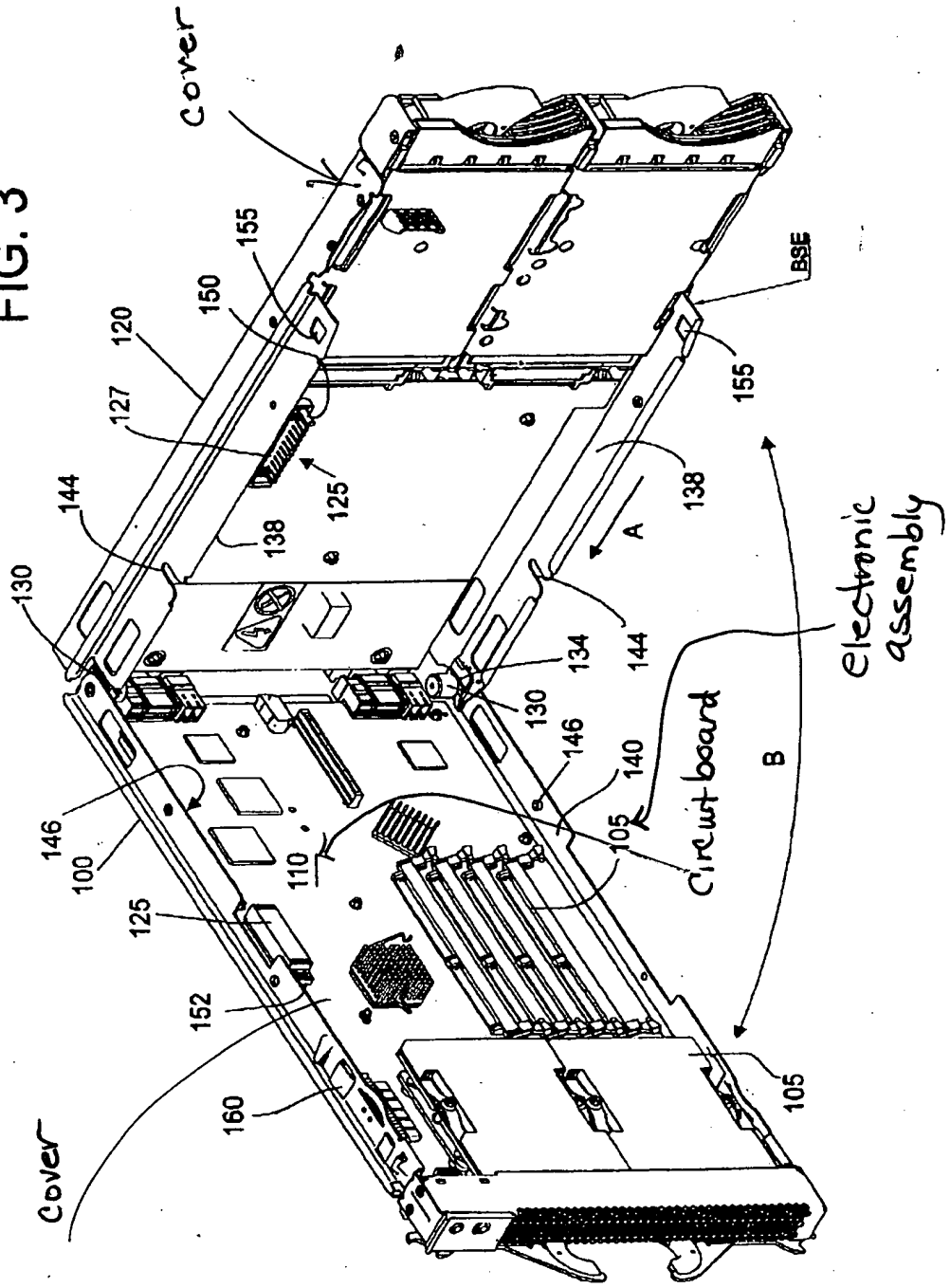

Cover
155
150
120
127
144
130
138
125
BSE
155
138
A
144
134
130
146
140
105
110
100
125
152
160
Cover
105
B
Circuit board
Electronic assembly

FIG. 9

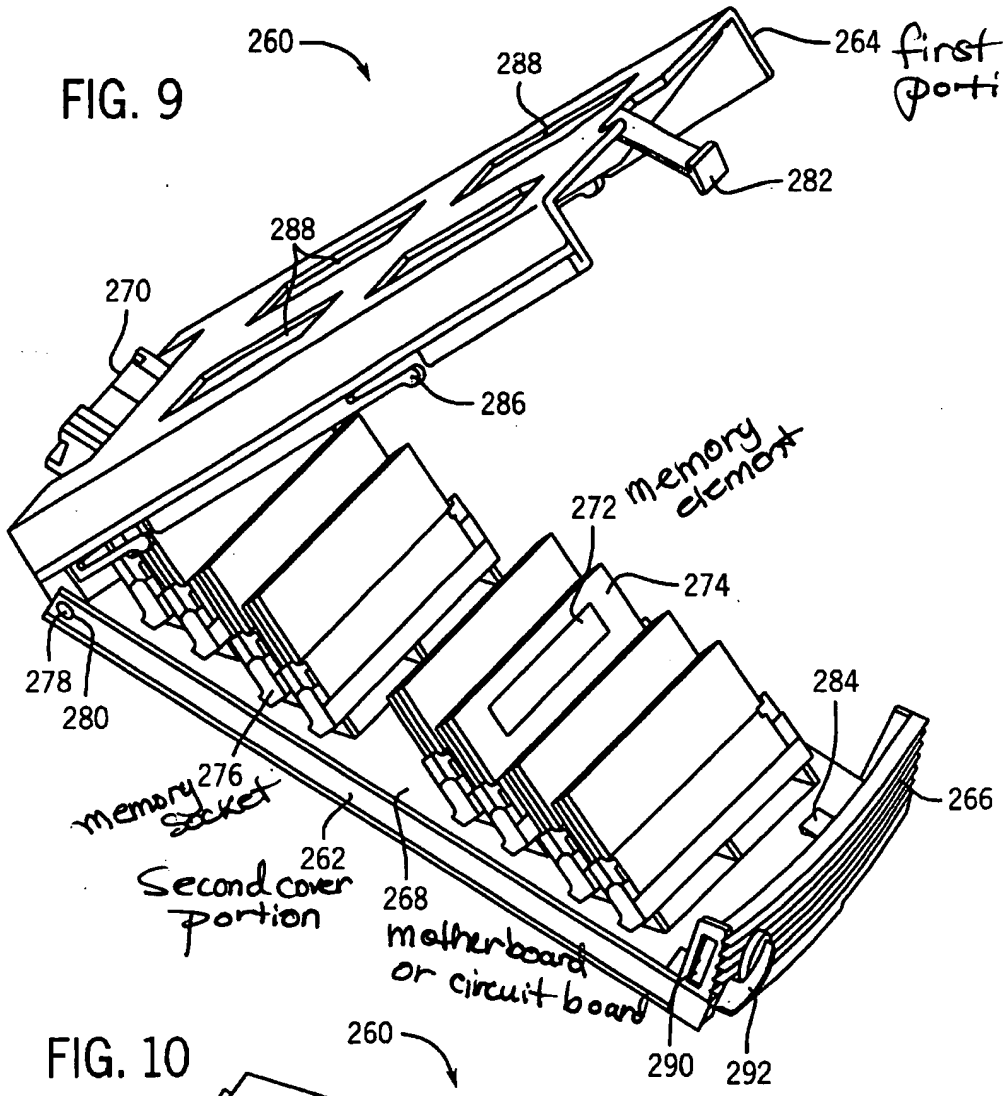
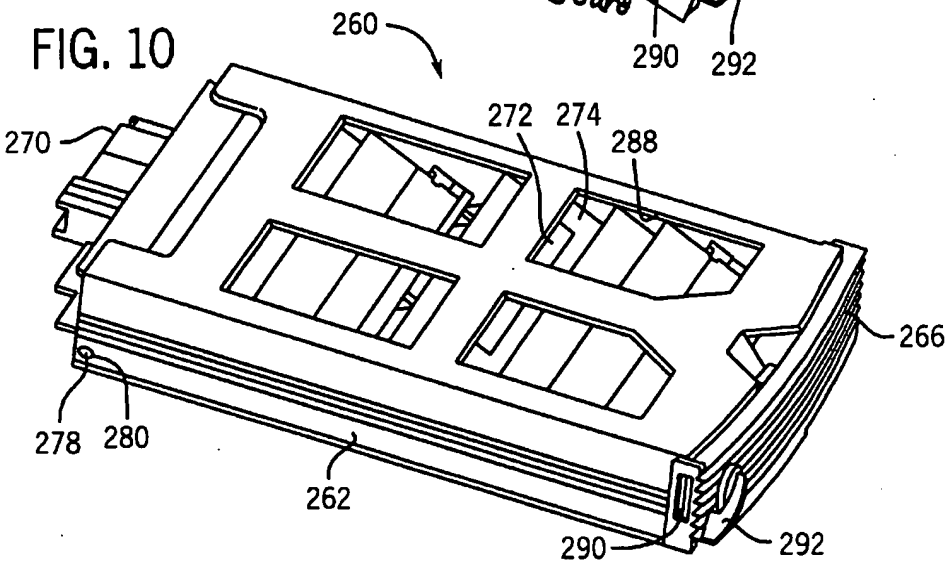

260
264
first cover portion
288
282
288
270
286
272
memory element
274
278
280
284
266
memory socket
276
262
Second cover portion
268
motherboard or circuit board
290
292

FIG. 10


260
270
272
274
288
266
278
280
262
290
292